Elias Kountouris

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Education

University of Waterloo 2021 - 2026
Candidate for Bachelor of Applied Science in Electrical Engineering GPA: 91.4%

Experience

UntetherAI - Physical Design Intern January 2025 - April 2025
- Implemented **fully custom SRAM array BL/WL drivers** using **Virtuoso** in **TSMC N5**
- Created **tcl** scripts to perform **PNR** on a timing sensitive, multi-supply block in **Innovus**
- Created custom level shifters, endcap, and welltap cells to reduce datapath area and power

UntetherAI - AI Accelerator Architecture Intern May 2024 - August 2024
- Designed the datapath and control logic for low-power, low-latency AI accelerators
- Designed and implemented a **SRAM controller** in Verilog to sequence read and write operations
- Designed and implemented a **DMA controller** in Verilog to request and load data from the NoC
- Completed timing closure of modules using **Synopsis Design Compiler**

University of Waterloo - Undergraduate Research Assistant May 2024 - Present
- Worked on a machine learning algorithm to perform transistor sizing on digital CMOS designs
- Modified open-source tools (COFFE and Yosys) to support FPGA architecture research
- Researched the viability of novel approaches for running embedded AI applications on FPGAs

Apple - iPhone Systems EE Intern September 2023 - December 2023
- Developed, assembled, and characterized **35 MHz power amplifier** to drive highly capacitive loads
- Researched and tested new methods to improve battery cell performance and longevity
- Performed early field failure analysis on iPhone 15s to identify common root causes of failure
- Debugged and tested the performance of prototype PCBs for future products

Microchip Technology - FPGA Engineering Intern January 2023 - August 2023
- Researched impacts on performance of high global routing usage for new FPGA fabrics
- Developed Python scripts to generate structural Verilog test designs to validate new CLB designs
- Resolved issues during test verification of new SoCs to help the team meet tapeout deadline

Projects

Dino Game ASIC - Verilog, Python, OpenROAD, OpenSTA
- Taped out custom ASIC for the Chrome Dino Game for Tiny Tapeout 10 using SKY130 process
- Designed pipelined rendering, collision and VGA graphics driver logic
- Used open source tools to perform PNR and STA to close design at 50 MHz

Bitcoin Mining on FPGA - SystemVerilog, Python, Vivado
- Designed fully pipelined SHA-256 encoder and state machine to compute Bitcoin hashes
- Created auto-generating test cases for each submodule using Cocotb, Verilator, and Python

Technical Skills

Virtuoso, Innovus, SPICE, SystemVerilog, Verilog, Tcl, Python, RISC-V, Linux, C++, C, Altium